

REMARKS

The Applicants thank Examiner Graybill for participating in the telephone interview with the Applicants' attorney on June 1, 2007.

Claims 2-5, 7, 9, 11-15, and 17 are withdrawn from consideration as being drawn to non-elected species.

With regard to the withdrawal of claims 2-5 and 7, Applicants request reconsideration of the withdrawal of claims 2-5 and 7. Specifically, claim 2 refers to a printed circuit board for a multi-chip package, which includes bonding pads to which a first connecting unit and a second connecting unit are connected, and pins for connecting the bonding pads to the external system. Applicants note that the term "pins" is generic to both pins of a BGA package and pins of a TQFP package of a printed circuit board, as would be readily known to one of ordinary skill in the art. For example, attached hereto is a publication entitled "Guidelines for Handling J-Lead, QFP & BGA Devices," by Altera Corporation, which is cited in the Supplemental Information Disclosure Statement filed concurrently with the current amendment. As shown in the cited publication at page 8, Table 5, the term "pins" is clearly shown as applying to pins of a BGA package and pins of a TQFP package.

In addition, claim 5 is amended herein to refer to a package type of the first semiconductor chip being a Wafer-Level Chip Size Package (W-CSP). New claim 19 is added herein to refer to a package type of the first semiconductor chip being a Fine Ball Grid Array (FBGA). Applicants note that new claim 19 is directed to a non-elected species pursuant to the Response to Species Election Requirement filed on December 13, 2006 in response to the Office Action dated November 16, 2006.

Therefore, it is submitted that claims 1-5 and 7 are in the elected species. Accordingly, reconsideration and removal of the withdrawal of claims 2-5 and 7 are respectfully requested.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Corisis (U.S. Patent Number 6,607,937) and Chang, *et al.* (United States Patent Application Publication Number 2002/0153599). In view of the amendments to the claims and the following remarks, reconsideration of the rejection of claim 1 is respectfully requested.

Independent claim 1 is amended herein to clarify certain features of the invention. Specifically, claim 1 is amended to clarify that a multi-chip package comprises a first semiconductor chip that includes a packaged flash memory. It is believed that this amendment made to claim 1 further clarifies the distinctions between the claimed invention and the cited references.

With regard to the rejection of claim 1, it is submitted Corisis and Chang, *et al.*, alone or in combination, fail to teach or suggest a first semiconductor chip that includes a packaged flash memory, as claimed in amended independent claim 1.

With regard to Corisis, there is no teaching or suggestion in Corisis of a multi-chip package comprising a first semiconductor chip that includes a packaged flash memory, as claimed in amended independent claim 1. Applicants note that the Office Action at page 4, second paragraph, refers to Corisis as not disclosing a first semiconductor chip that includes a flash memory.

With regard to Chang, *et al.*, Chang, *et al.* teaches a bottom chip 21 that can be one kind of memory chip, for example, flash memory (see Chang, page 2, paragraph [0009]). However, there is likewise no teaching or suggestion in Chang, *et al.* of the bottom chip 21 of Chang, *et al.* including a packaged flash memory, as claimed in amended independent claim 1. Instead, the bottom chip 21 of Chang, *et al.* is an unpackaged flash memory.

Applicants note that, although the multi-chip package 20 of Chang, *et al.* includes a package body 28, in which the bottom chip 21 is positioned, this is different than a packaged flash memory, as claimed in claim 1. Instead, as stated above, the bottom chip 21 of Chang, *et al.* is an unpackaged flash memory. Further, the bottom chip 21 includes bonding wires 26 connected to bonding pads of the bottom chip 21, similar to the conventional semiconductor chip 110, which, like Chang, *et al.*, is a bare chip, or unpackaged chip, described in the Background of the Invention section of the present specification. Accordingly, since the bottom chip 21 of Chang, *et al.* is similar to the semiconductor chip 110 described in the Background of the Invention section of the present specification, Applicants further submit that the bottom chip 21 of Chang, *et al.* suffers limitations similar to those described in the Background of the Invention section of the present specification.

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It is therefore submitted that Corisis and Chang, *et al.*, alone or in combination, fail to teach or suggest elements of the invention set forth in claim 1. Specifically, Corisis and Chang, *et al.* fail to teach or suggest a multi-chip package comprising a first semiconductor chip that includes a packaged flash memory, as claimed in amended independent claim 1. Accordingly, there is no combination of Corisis and Chang, *et al.* which would provide such teaching or suggestion.

Since the combination of Corisis and Chang, *et al.* fails to teach or suggest the invention set forth in the amended claims, the claims are believed to be allowable over the cited references. Accordingly, reconsideration and removal of the rejection of claim 1 under 35 U.S.C. 103(a) based on the combination of Corisis and Chang, *et al.* are respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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